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For: METHODS OF FABRICATING A SEMICONDUCTOR DEVICE HAVING  
MULTI-GATE INSULATION LAYERS AND SEMICONDUCTOR DEVICES  
FABRICATED THEREBY

INFORMATION DISCLOSURE CITATION  
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Document</u> <u>Number</u>	<u>Issue</u> <u>Date</u>	<u>Name</u>	<u>Class</u>	<u>Sub</u> <u>Class</u>
<u>MEW</u>		US 6,222,225 B1	4/24/2001	Nakamura, et al.		

Examiner: Matthew E. Warner

Date Considered: 3/13/05